AMENDMENTS TO THE DRAWINGS

Figure 3 is being amended to remove the Prior Art legend which was inadvertently included on the figure when the formal drawings were submitted.

Attachments: Annotated Sheet

Replacement Sheet

REMARKS

Claims 1-17 are pending in the application. Figure 3 has been amended.

Figure 3 has been amended to remove the Prior Art legend that was inadvertently included on the figure when the formal drawings were submitted. The figure as originally filed did not include the Prior Art legend. Applicants point the Examiner to pages 5-6 of the specification to illustrate that Figure 3 is not prior art. Specifically, the specification recites "FIG. 3 illustrates an exemplary DRAM circuit 200 according to an embodiment of the present invention." Accordingly, Applicants request that the Examiner enter the amendment to Figure 3.

Claims 1-17 stand rejected under 35 U.S.C. §102 (b) as being anticipated by U.S. Patent No. 5,457,661 to Yomita et al. ("Yomita"). Applicants respectfully request withdrawal of the rejection.

The invention claimed in claims 1-17 is directed to improving power consumption and memory access speed in DRAM circuits by controlling and sensing shorter data lines before the longer data lines. In an embodiment of the invention the delay circuit is comprised of multiple delay devices which control the timing of when data is received and sensed by the data sense amplifiers. The delay circuit, having multiple delay devices, produces varying delay times for longer and shorter data lines.

Claim 1 recites, inter alia, "transferring data from a memory module onto an input/output signal line; and sensing the data based on a capacitance of said input/output signal line."

Yomita teaches a column output delay circuit within each decoder which senses all of the lines corresponding to the decoder simultaneously. However, Yomita does mention or teach a column output circuit for "sensing the data based on a capacitance

of said input/output signal line." Accordingly, all of the limitations of independent claim 1 are not taught by Yomita. Applicants respectfully request withdrawal of the rejection of independent claims 1 and depending claims 2-5 for at least the above-mentioned reasons.

Claim 6 recites a "column output delay circuit for a memory device comprising: a first delay device, said first delay device delaying a column enable signal for a first period of time; and a second delay device, said second delay device delaying a column enable signal for a second period of time."

Claim 6 is directed to a column output delay circuit in which there is a first and second delay device. Conversely, Yomita teaches a plurality of column output decoders in which each decoder may have a delay circuit. The delay circuits, of each decoder, taught in Yomita do not have "a first delay device, said first delay device delaying a column enable signal for a first period of time; and a second delay device, said second delay device delaying a column enable signal for a second period of time." Accordingly, as Yomita fails to each every limitation of claim 6, Applicants respectfully request withdrawal of the rejection. For at least the reasons mentioned above, Applicants respectfully request the rejection of depending claims 7-8 be withdrawn.

Claims 9 and 14 recite, inter alia, "a datapath coupled to said memory array by input/output signal lines, and a column output delay circuit, said circuit coupled to sense amplifiers in said datapath for controlling, based on a capacitance of a particular input/output signal line, when the particular input/output signal line is sensed by said sense amplifiers."

Yomita fails to teach a column output delay circuit for controlling when a particular input/output line is sensed. Instead, Yomita teaches a first stage column

decoder and a second stage column decoder in which a sense signal is supplied to a latch circuit. As the latch circuit receives the sense signal, a decode signal is applied to the gates of the first and second stage column decoders. The inverters within the decoders provide the same delay to all of the connected data lines. The inverter delay circuits of the different decoders may provide varying delays. Yomita does not teach a "a column output delay circuit, said circuit coupled to sense amplifiers in said datapath for controlling, based on a capacitance of a particular input/output signal line, when the particular input/output signal line is sensed by said sense amplifiers." Accordingly, all of the limitations of independent claims 9 and 14 are not taught by Yomita. Applicants respectfully request withdrawal of the rejection of independent claims 9 and 14 and depending claims 10-13 and 15-17, respectfully, for at least the above-mentioned reasons.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

By_____

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